

### Abstract of the Disclosure

An improved Flash memory device is described with a protection register lock bit erase enable circuit. A bond pad coupled to the lock bit erase enable circuit of the improved Flash memory is not bonded when the individual Flash memory chip wafer is packaged. This allows the memory manufacturer to access the bond pad and erase the lock bits while the chip is still in wafer form via a test card probe, but makes the lock bits effectively uneraseable when the chip wafer is packaged. This enables the memory chip manufacturer to enhance reliability and fault tolerance of the Flash memory device by thoroughly testing the lock bits and protection register functionality. Additionally, the lock bit erase enable circuit increases manufacturing flexibility by allowing the memory chip manufacturer to reprogram the protection register and lock bits in case of organizational changes or inadvertent or erroneous programming of the protection register.